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(54) **LARGE MULTIPLIER FOR PROGRAMMABLE LOGIC DEVICE**

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G06F 7/53 (2006.01)
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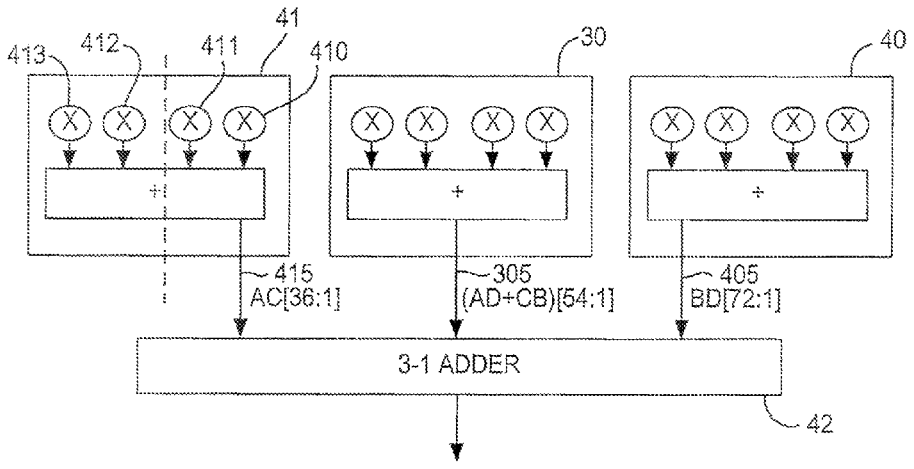
(57) **ABSTRACT**

A plurality of specialized processing blocks in a programmable logic device, including multipliers and circuitry for adding results of those multipliers, can be configured as a larger multiplier by adding to the specialized processing blocks selectable circuitry for shifting multiplier results before adding. In one embodiment, this allows all but the final addition to take place in specialized processing blocks, with the final addition occurring in programmable logic. In another embodiment, additional compression and adding circuitry allows even the final addition to occur in the specialized processing blocks. Circuitry that controls when an input is signed or unsigned facilitates complex arithmetic.

21 Claims, 9 Drawing Sheets



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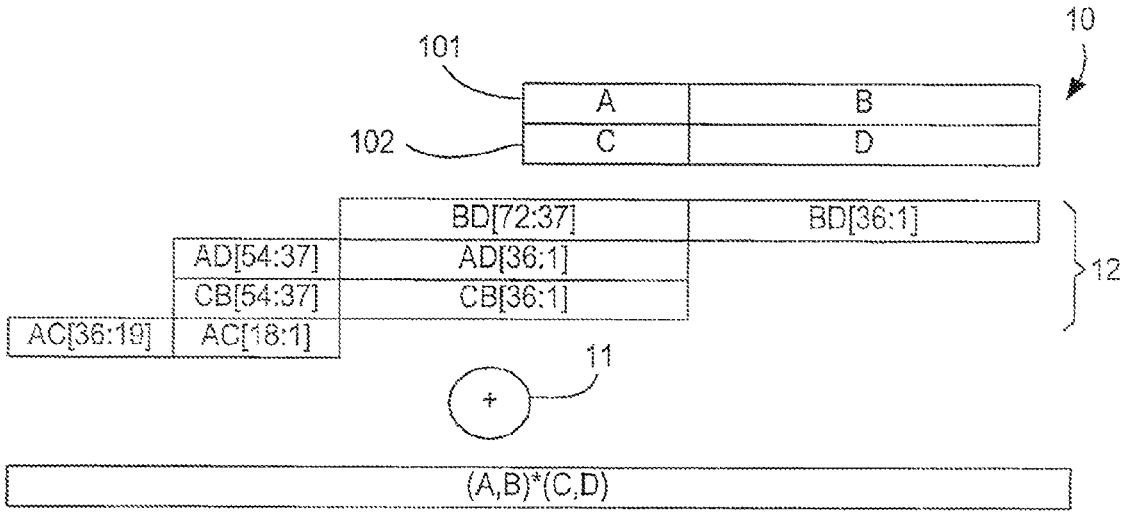
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102
C
D
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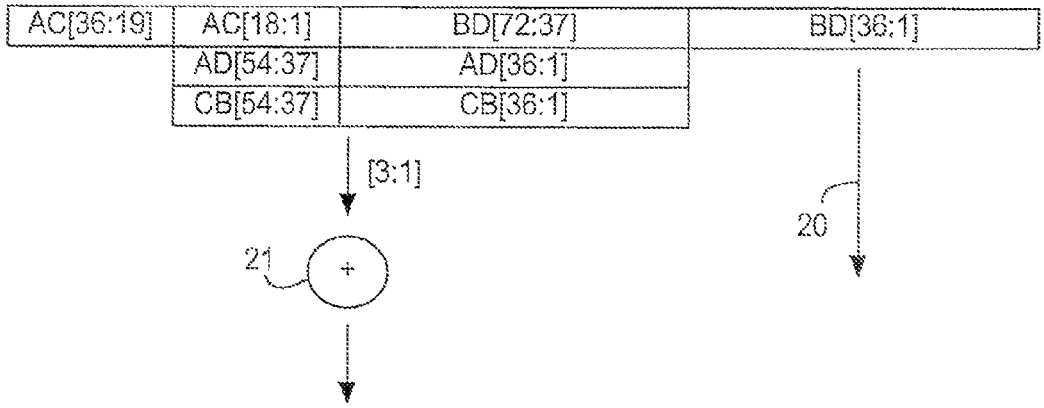
AD[54:37]
AD[36:1]
CB[54:37]
CB[36:1]
12
AC[36:19]
AC[18:1]
11
+
(A,B)*(C,D)

FIG. 1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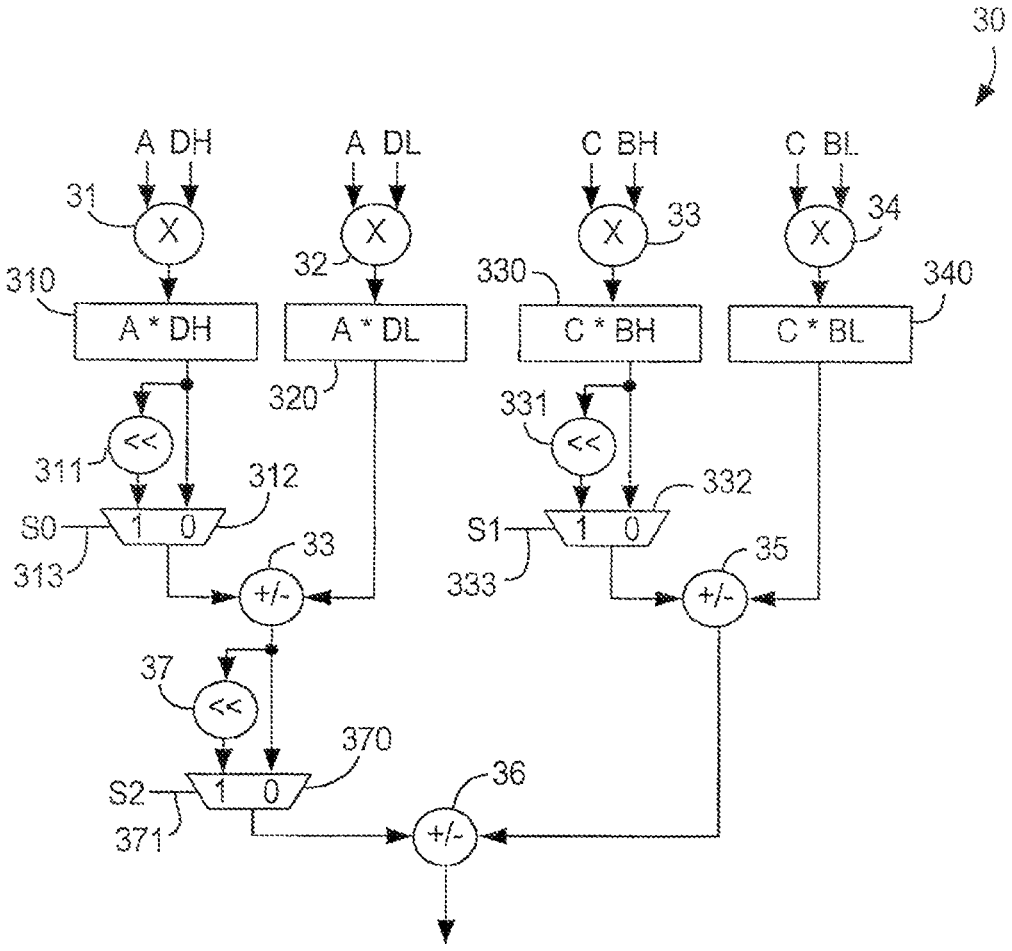
21
+

FIG. 2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C BH
C BL
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33
34
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320
330
340
A * DH
A * DL
C * BH
C * BL
<<
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312
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S1
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S2
371
36

FIG. 3

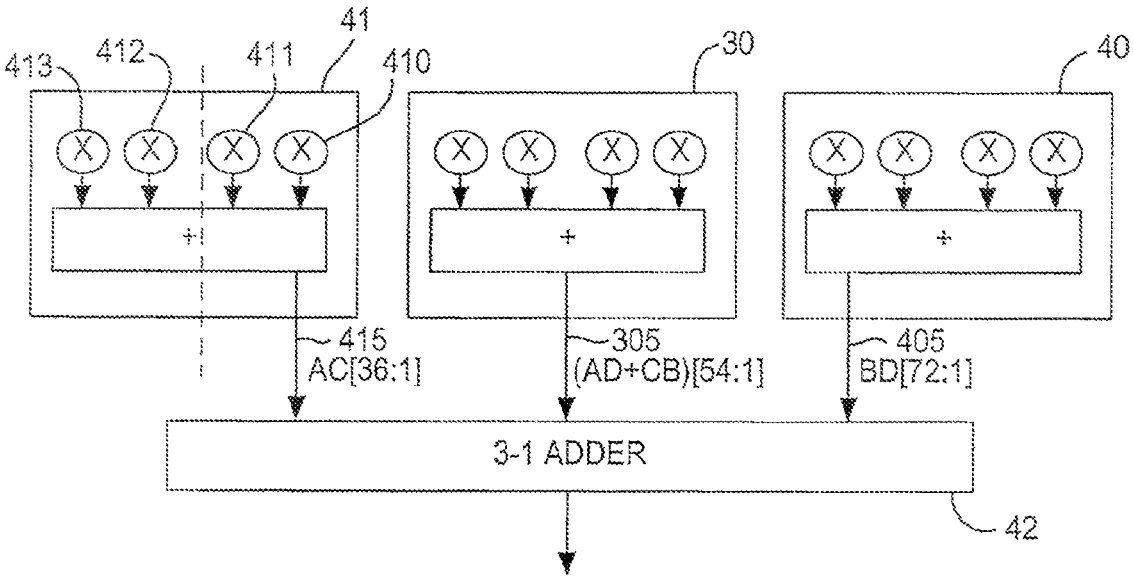
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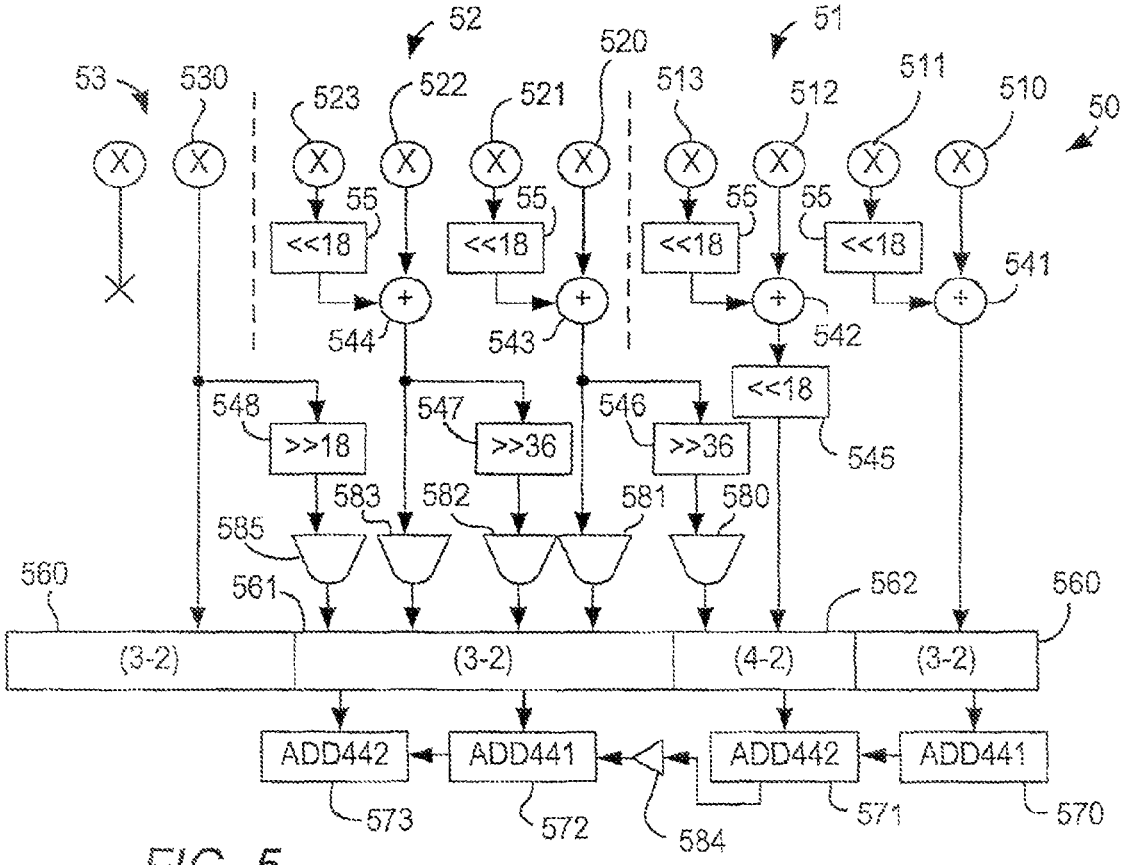
FIG. 4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546
>>18
>>36
545
583
582
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(4-2)
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ADD441
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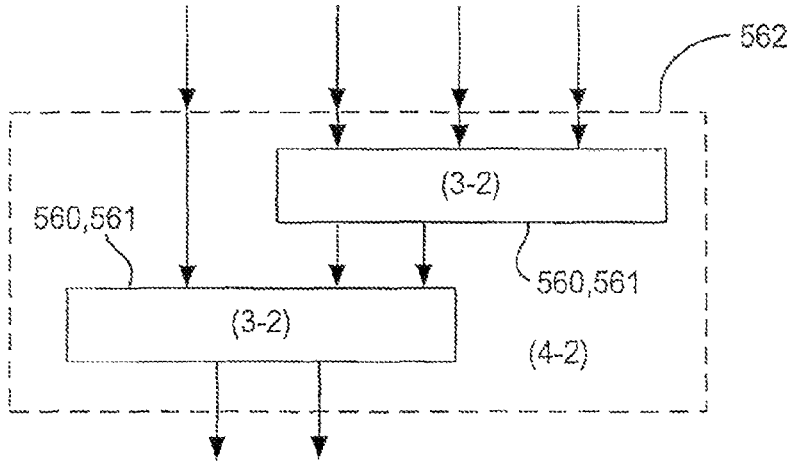
571
570

FIG. 5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(4-2)

FIG. 6

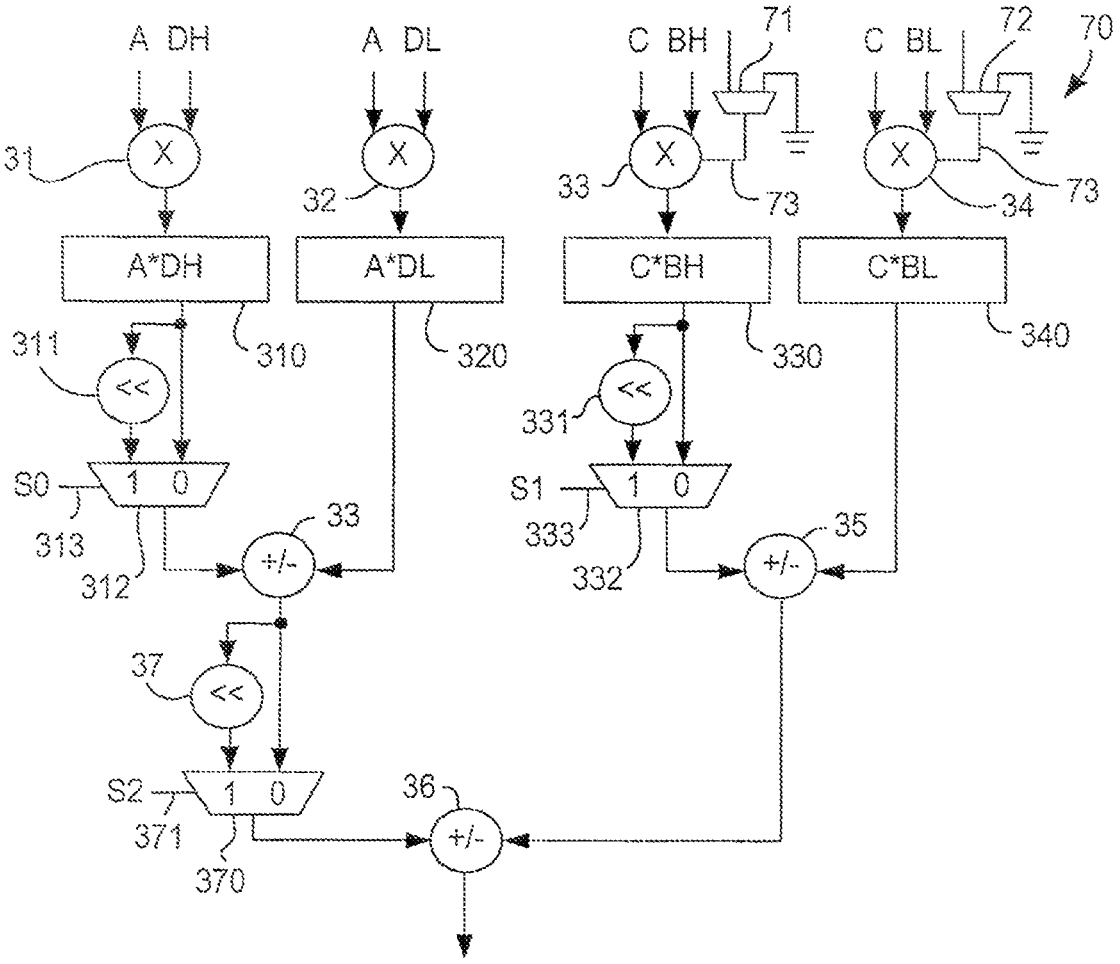
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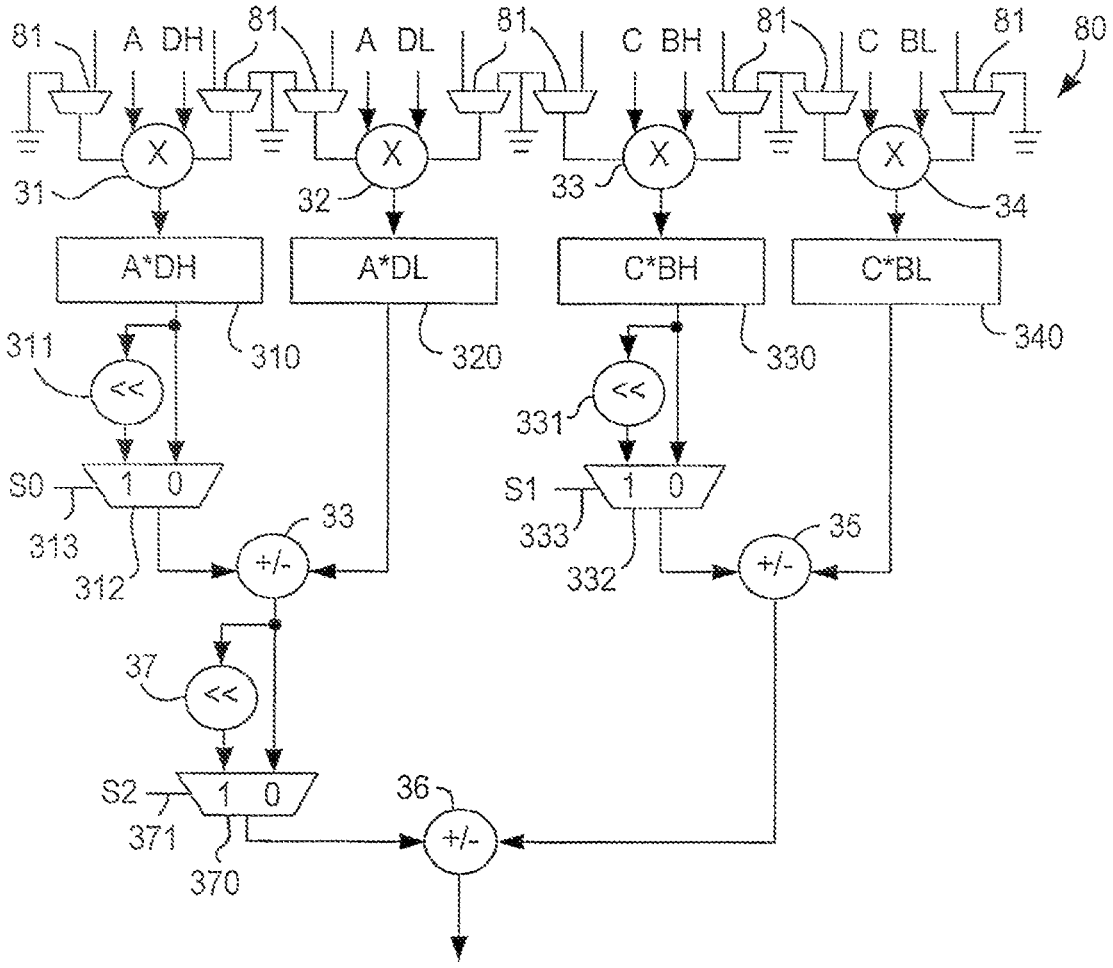
FIG. 7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A*DL
C*BH
C*BL
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331
S0
1 0
S1
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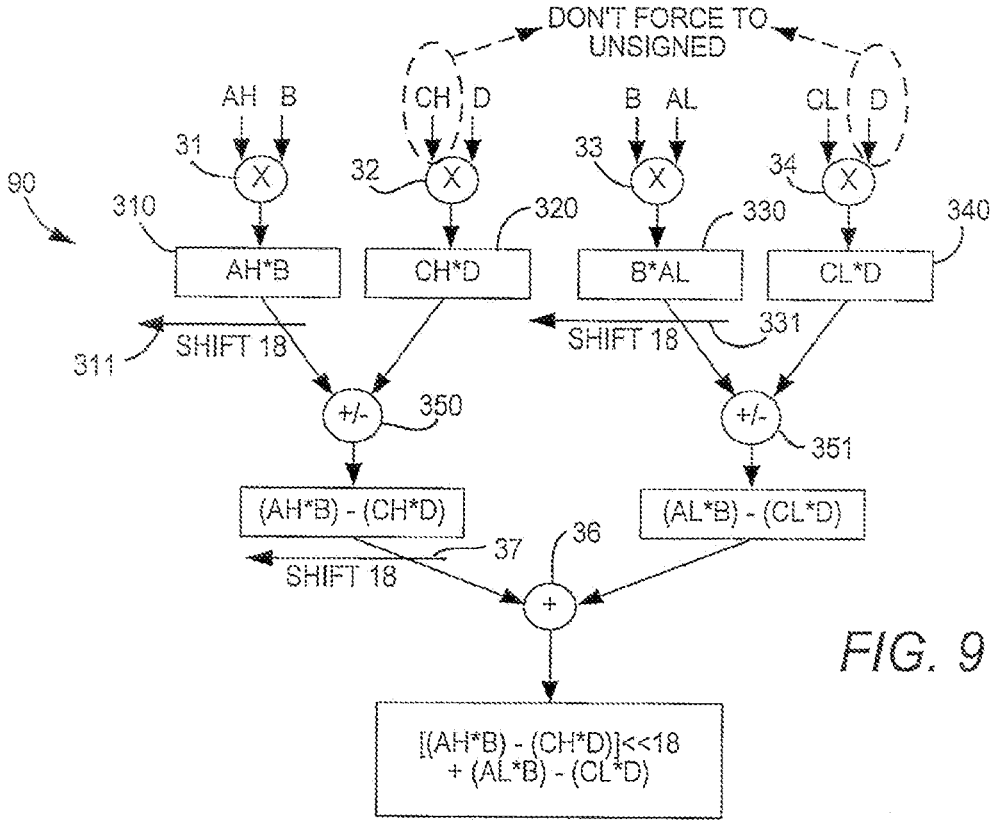
+/-

FIG. 8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CH D
B AL
CL D
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90
310
320
330
340
AH*B
CH*D
B*AL
CL*D
SHIFT 18
SHIFT 18
311
331
+/-
+/-
350
351
(AH*B) - (CH*D)
(AL*B) - (CL*D)
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SHIFT 18
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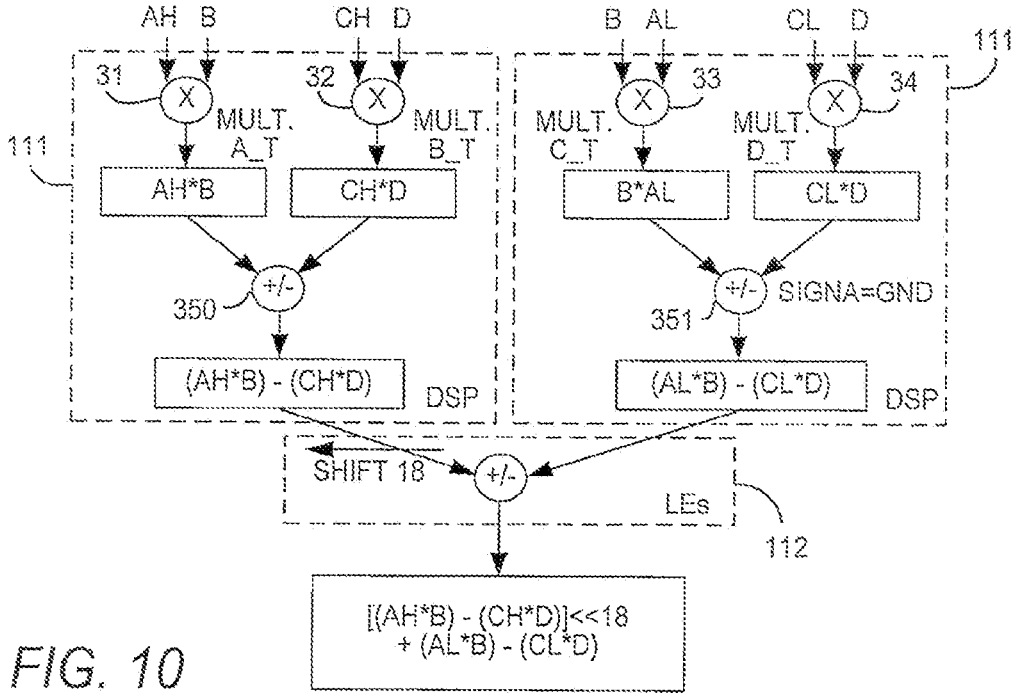
+ (AL*B) - (CL*D)

FIG. 9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CH D
B AL
CL D
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MULT. B_T
MULT. C_T
MULT. D_T
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AH*B
CH*D
B*AL
CL*D
+/-
+/-
SIGNA=GND
350
351
(AH*B) - (CH*D)
(AL*B) - (CL*D)
DSP
DSP
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LEs
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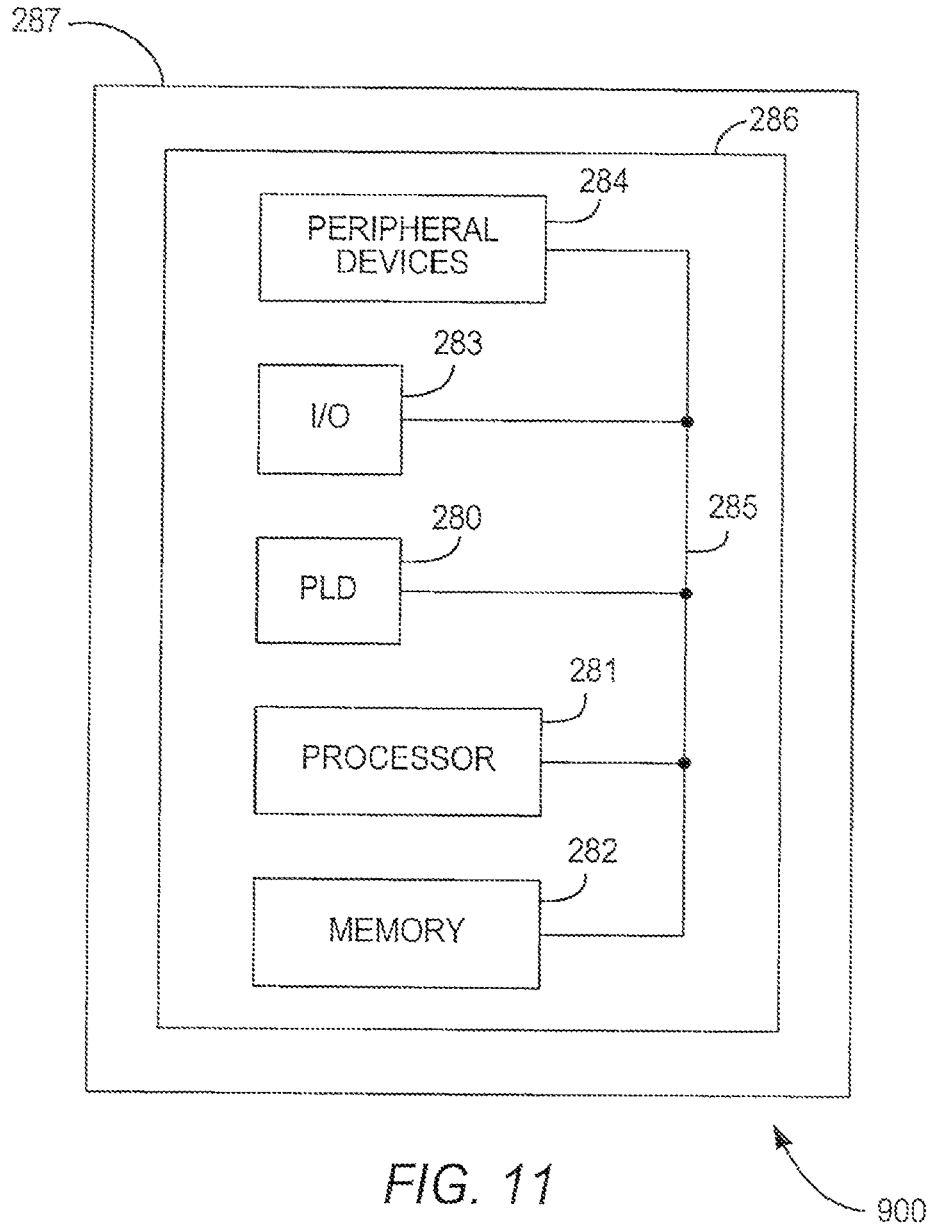
+ (AL*B) - (CL*D)

FIG. 10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MEMORY
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FIG. 11

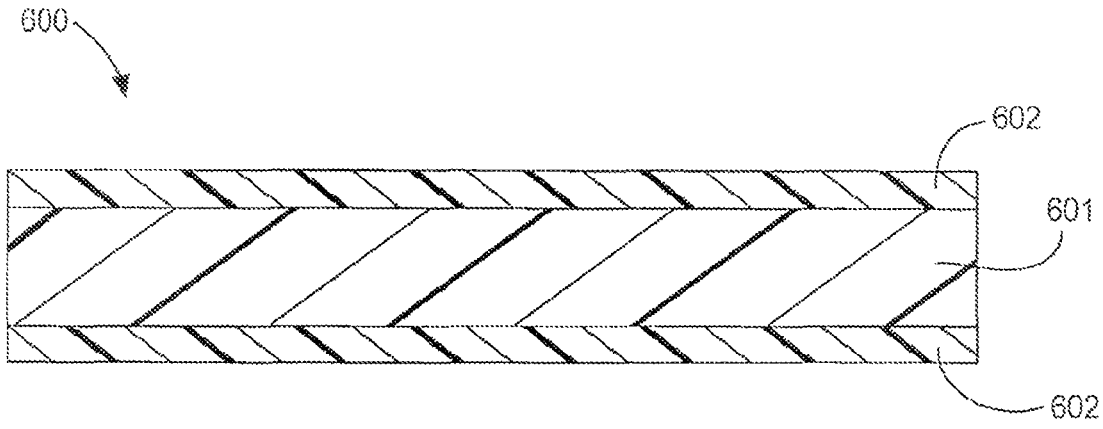

FIG. 12

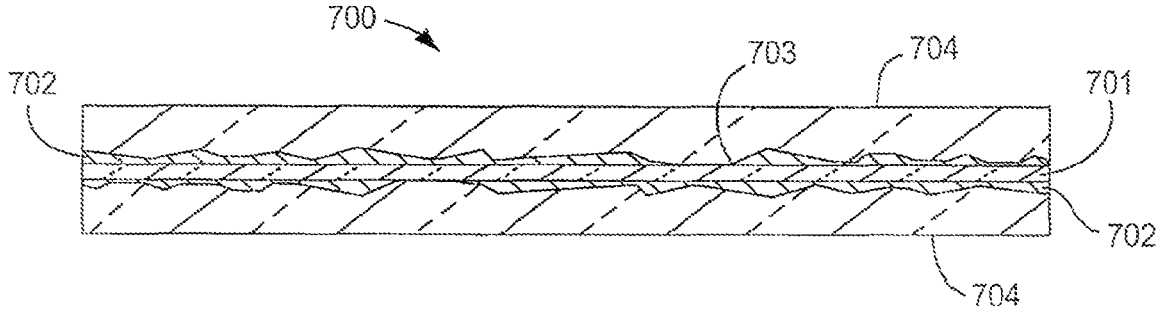

FIG. 13

LARGE MULTIPLIER FOR PROGRAMMABLE LOGIC DEVICE

CROSS REFERENCE TO RELATED APPLICATION

This is a division of commonly-assigned U.S. patent application Ser. No. 11/682,787, filed Mar. 6, 2007, now U.S. Pat. No. 8,386,553, which is a continuation-in-part of commonly-assigned U.S. patent application Ser. No. 11/566,982, filed Dec. 5, 2006 and copending therewith, each of which is hereby incorporated by reference herein in its respective entirety.

BACKGROUND OF THE INVENTION

This invention relates to programmable logic devices (PLDs), and, more particularly, to the use of specialized processing blocks which may be included in such devices to perform large multiplications.

As applications for which PLDs are used increase in complexity, it has become more common to design PLDs to include specialized processing blocks in addition to blocks of generic programmable logic resources. Such specialized processing blocks may include a concentration of circuitry on a PLD that has been partly or fully hardwired to perform one or more specific tasks, such as a logical or a mathematical operation. A specialized processing block may also contain one or more specialized structures, such as an array of configurable memory elements. Examples of structures that are commonly implemented in such specialized processing blocks include: multipliers, arithmetic logic units (ALUs), barrel-shifters, various memory elements (such as FIFO/LIFO/SIPO/RAM/ROM/CAM blocks and register files), AND/NAND/OR/NOR arrays, etc., or combinations thereof.

One particularly useful type of specialized processing block that has been provided on PLDs is a digital signal processing (DSP) block, which may be used to process, e.g., audio signals. Such blocks are frequently also referred to as multiply-accumulate ("MAC") blocks, because they include structures to perform multiplication operations, and sums and/or accumulations of multiplication operations.

For example, a PLD sold by Altera Corporation, of San Jose, Calif., under the name STRATIX® II includes DSP blocks, each of which includes four 18-by-18 multipliers. Each of those DSP blocks also includes adders and registers, as well as programmable connectors (e.g., multiplexers) that allow the various components to be configured in different ways. In each such block, the multipliers can be configured not only as four individual 18-by-18 multipliers, but also as four smaller multipliers, or as one larger (36-by-36) multiplier. In addition, one 18-by-18 complex multiplication (which decomposes into two 18-by-18 multiplication operations for each of the real and imaginary parts) can be performed.

Although such a DSP block may be configured as a multiplier as large as 36-by-36, a user may want to create a larger multiplier. For example, while a 36-by-36 multiplier will support 25-by-25 single-precision multiplication under the IEEE 754-1985 standard, it is too small for double-precision multiplication, or for 36-by-36 complex multiplication. While the multipliers from several DSP blocks can be used together to implement double-precision multiplication, or larger complex multiplication, the logic needed to interconnect the multipliers has heretofore been programmed by the user in the general-purpose programmable logic outside the DSP block, making it slow and less efficient, and consuming general-purpose resources that might be put to other uses.

SUMMARY OF THE INVENTION

The present invention relates to specialized processing blocks for PLDs that are provided with logic within the blocks to facilitate the performance of multiplications larger than that which can be performed within any single specialized processing block, reducing or eliminating reliance on general-purpose programmable resources of the PLD.

In accordance with the invention, control is provided over whether one or more multiplicand inputs are forced to be unsigned or are allowed to be signed. This enables the performance of more of the calculations involved in signed or complex multiplications. The ability to shift results—either within or outside the block—before further processing, further increases the number of types of calculations that can be performed.

In accordance with the present invention, there is provided, for use in a programmable logic device having a plurality of specialized processing blocks, each of those specialized processing blocks having at least four n-by-n multipliers arranged in four-multiplier units, a method of performing a signed 3n-by-3n multiplication operation. The method includes performing a 2n-by-2n multiplication using four of the n-by-n multipliers in a first of the four-multiplier units, performing an n-by-n multiplication using one of the n-by-n multipliers in a second of the four-multiplier units, and performing first and second 2n-by-n multiplications in a third of the four-multiplier units, using two of the n-by-n multipliers for each of the 2n-by-n multiplications. In each of the multiplications, multiplicands representing n most significant bits are treated as signed operands and multiplicands representing n least significant bits are forced to be unsigned. The method further includes shifting a second partial product of each of the 2n-by-n multiplications to align it with a first partial product of each of the 2n-by-n multiplications for addition within the third four-multiplier unit, and adding results of the multiplications from the first, second and third four-multiplier units.

A programmable logic device configured to perform the method, and software to configure the programmable logic device, are also provided.

In addition, there is provided a method of performing a complex 2n-by-n multiplication operation in such a programmable logic device. The method includes

(a) computing an imaginary part of the complex multiplication in a first of the four-multiplier units by (1) breaking each of real and imaginary parts of a 2n-bit multiplicand into respective upper and lower n-bit portions, (2) performing first respective n-by-n multiplications of upper and lower n-bit portions of the real part of the 2n-bit multiplicand by an imaginary part of the n-bit multiplicand using a first two of the four multipliers of the first four-multiplier unit, shifting a result of the first respective multiplication involving the upper portion relative to a result of the first respective multiplication involving the lower portion, and adding the first respective multiplications to form a first partial product, (2) performing second respective n-by-n multiplications of upper and lower n-bit portions of the imaginary part of the 2n-bit multiplicand by a real part of the n-bit multiplicand using a second two of the four multipliers of the first four-multiplier unit, shifting a result of the second respective multiplication involving the upper portion relative to a result of the second respective multiplication involving the lower portion, and adding the second respective multiplications to form a second partial

product, and (3) adding the first and second partial products; and (b) computing a real part of the complex multiplication in a second of the four-multiplier units by (1) performing a first n-by-n multiplication of the upper n-bit portion of the real part of the 2n-bit multiplicand by the real part of the n-bit multiplicand using a first of the four multipliers of the second four-multiplier unit, performing a second n-by-n multiplication of the upper n-bit portion of the imaginary part of the 2n-bit multiplicand by the imaginary part of the n-bit multiplicand using a second of the four multipliers of said second four-multiplier unit, and performing a first subtraction of a result of the second multiplication from the result of the first multiplication to form a third partial product, (2) performing a first n-by-n multiplication of the lower n-bit portion of the real part of the 2n-bit multiplicand by the real part of the n-bit multiplicand using a third of the four multipliers of the second four-multiplier unit, performing a fourth n-by-n multiplication of the lower n-bit portion of the imaginary part of the 2n-bit multiplicand by the imaginary part of the n-bit multiplicand using a fourth of the four multipliers of the second four-multiplier unit, and performing a first subtraction of a result of the second multiplication from said result of the first multiplication to form a fourth partial product, (3) shifting a result of the third partial product relative to the fourth partial product, and (4) adding the third partial product to the fourth partial product.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and advantages of the invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

FIG. **1** is a representation of the decomposition of a 54-bit-by-54-bit multiplication into a sum of partial products;

FIG. **2** is a representation of the alignment of the partial products of FIG. **1** for addition;

FIG. **3** is schematic representation of a portion of a specialized processing block for use in a first preferred embodiment of the present invention;

FIG. **4** is a schematic representation of the performance of a 54-bit-by-54-bit multiplication in a preferred embodiment of the present invention;

FIG. **5** is a schematic representation of a group of specialized processing blocks for use in another preferred embodiment of the present invention;

FIG. **6** is a schematic representation of a 4:2 compressor used in the embodiment of FIG. **5**;

FIG. **7** is a schematic representation of a portion of a specialized processing block configured to perform part of a 36-bit-by-18-bit complex multiplication in another preferred embodiment of the present invention;

FIG. **8** is schematic representation of another preferred embodiment of the portion of the specialized processing block of FIG. **7**;

FIG. **9** is a schematic representation of a portion of a specialized processing block configured to perform the real part of a 36-bit-by-18-bit complex multiplication in another preferred embodiment of the present invention;

FIG. **10** is a schematic representation of the performance of a portion of a 36-bit-by-17-bit complex multiplication in accordance with another embodiment of the present invention;

FIG. **11** is a simplified block diagram of an illustrative system employing a programmable logic device incorporating the present invention;

FIG. **12** is a cross-sectional view of a magnetic data storage medium encoded with a set of machine-executable instructions for performing the method according to the present invention; and

FIG. **13** is a cross-sectional view of an optically readable data storage medium encoded with a set of machine executable instructions for performing the method according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention will now be described with reference to FIGS. **1-6** in the context of a 54-bit-by-54-bit multiplication, which maps well onto the 18-bit multipliers of the DSP block of the aforementioned STRATIX® II PLD, and which can be used to implement double-precision multiplication under the IEEE 754-1985 standard. However, the invention can be used with specialized processing blocks of different sizes.

FIG. **1** shows the decomposition of a 54-bit-by-54-bit multiplication **10** into a sum **11** of partial products **12** that can be implemented using 18-bit-by-18-bit multipliers to yield product **13**. In the first multiplicand **101**, A contains the 18 most significant bits, and B contains the 36 least significant bits. In the second multiplicand **102**, C contains the 18 most significant bits, and C contains the 36 least significant bits. The result (A,B)×(C,D) can be calculated as B×D+((A×D+C×B)<<36)+((A×C)<<72), where "<<n" indicates that the result of the expression to which it relates is shifted to the left by n places.

The intermediate values required for a floating point mantissa multiplication preferably are unsigned when performing a 54-bit multiplication—i.e., they include a 52-bit mantissa preceded by "01." The intermediate values can be aligned as in FIG. **2**, providing as outputs 36-bit output 20 and 3-level 72-bit addition **21**.

In the DSP block of the aforementioned STRATIX® II PLD, as well as in an improved DSP block described in copending, commonly-assigned U.S. patent application Ser. Nos. 11/447,329, 11/447,370, 11/447,472, 11/447,474, all filed Jun. 5, 2006, Ser. No. 11/426,403, filed Jun. 26, 2006, and Ser. No. 11/458,361, filed Jul. 18, 2006, each of which is hereby incorporated herein in its respective entirety, four multipliers are arranged in a unit, which may be referred to as a block or a half-block, along with compressors, adders, shifters and multiplexers, to form and add the various partial products.

As applied to the current problem illustrated in FIGS. **1** and **2**, that DSP block architecture can support the 36-bit-by-36-bit multiplication (B×D) and the 18-bit-by-18-bit multiplication (A×C), but the multiplexer pattern of that architecture cannot support the connections necessary to add together the two 18-bit-by-36-bit multiplications (A×D and C×B). Each of the 18-bit-by-36-bit multiplications is supported individually, but the results must be routed out of the DSP block, and added in the general-purpose programmable logic of the PLD. This consumes a large amount of general-purpose programmable logic as well as routing and interconnect resources.

In accordance with the present invention, the intermediate multiplexer arrangement of the DSP block is changed, as compared to the aforementioned DSP block, in a manner that allows the sum of two 18-bit-by-36-bit multiplications to be produced in a single four-multiplier block/half-block. As a result, all of the partial products necessary for a 54-bit-by-54-bit multiplication can be performed and at least partially summed together within a single four-multiplier block/half-block.

In a first preferred embodiment illustrated in FIGS. **3** and **4**, for a pair of multiplicands A and D, D may be split into most significant and least significant halves, or DH and DL. The product A×D can then be expressed as (A×DH)<<18+A×DL. (A×DH) preferably is provided at **310** by multiplier **31**, and is then shifted left 18 bits by shifter **311**, selected by multiplexer **312** under control of signal **313**. A×DL preferably is provided at **320** by multiplier **32**. The product A×D is then preferably provided by adding partial products **310** and **320** at adder **350**, which may include a 4:2 compressor, and a 30-bit adder and a 24-bit adder concatenated together (not shown).

A second pair of multiplicands C and B can be treated similarly to provide (C×BH)<<18+C×BL. (C×BH) preferably is provided at **330** by multiplier **33**, and is then shifted left 18 bits by shifter **331**, selected by multiplexer **332** under control of signal **333**. C×BL preferably is provided at **340** by multiplier **34**. The product C×B is then preferably provided by adding partial products **330** and **340** at adder **351**, which may include a 4:2 compressor, and a 30-bit adder and a 24-bit adder concatenated together (not shown).

The two 54-bit sums of the 18-bit-by-36-bit multiplications A×D and C×B preferably are then added together at adder **36**, which may include a 4:2 compressor, and two 44-bit adders concatenated together (not shown). Although a 18-bit shifter **37** is provided for selectively left-shifting the output of adder **33** as selected by multiplexer **370** under control of signal **371**, for the purpose of this 54-bit addition, sum **33** (A×D) is not shifted.

Specifically, the three shifters **311**, **331**, **37**, under control of signals **312**, **332**, **371**, allows specialized processing block **30** to be used for multiple functions. For example, for a sum of four 18-bit-by-18-bit multiplications, each of signals **312**, **332**, **371** preferably is set to select its respective unshifted result. For a single 36-bit-by-36-bit multiplication, each of signals **312**, **332**, **371** preferably is set to select its respective shifted result. And as already stated, for performing the two 18-bit-by-36-bit partial products of a 54-bit-by-54-bit multiplication, each of signals **312**, **332** preferably is set to select its respective shifted result, while signal **371** preferably is set to select its unshifted result.

As seen in FIG. **4**, the 54-bit-by-54-bit multiplication is performed by using specialized processing block/half-block **40** to perform the 36-bit-by-36-bit partial product B×D, using specialized processing block/half-block **30** to perform and sum the two 18-bit-by-36-bit partial products A×D and C×B, and using specialized processing block/half-block **41** to perform the single 18-bit-by-18-bit multiplication A×C. Note that only one of the four multipliers **410**-**413** in block/half-block **41** is used, although as explained in above-incorporated application Ser. No. 11/447,472, if block/half-block **41** is the one described in that application, using only one multiplier **410** requires sacrificing a second multiplier **411**. However, in that embodiment, at least multipliers **412**, **413** remain available for other purposes, and in other embodiments even multiplier **411** may be available.

In accordance with the embodiment of the present invention depicted in FIGS. **3** and **4**, the three partial products or sums of partial products **405**, **305** and **415** are added by adder **42**, which preferably is created outside the specialized processing blocks **40**, **30**, **41** in programmable logic of the PLD of which specialized processing blocks **40**, **30**, **41** are a part.

In the embodiment of FIGS. **3** and **4**, it is still necessary to use general-purpose programmable logic, routing and interconnect resources for the final addition **42**. In a second preferred embodiment **50** shown in FIG. **5**, a 54-bit-by-54-bit multiplication can be performed substantially entirely in specialized processing blocks on a PLD, substantially without resort to the general-purpose programmable logic of that PLD. In embodiment **50**, preferably two four-multiplier units **51**, **52** and a portion of third four-multiplier unit **53** are used. Preferably, each of these four-multiplier units **51**-**53** is based on half-blocks of the specialized processing block described in above-incorporated application Ser. No. 11/447,472, modified as described herein. Thus, a full one such block and a portion of a second such block preferably are used.

In embodiment **50**, each half-block **51**, **52** (and half-block **53**, but not all components are shown because only one multiplier **530** is used from that half-block **53**) preferably has four 18-bit-by-bit multipliers **510**-**513**, **520**-**523**, preferably arranged in pairs **510**-**511**, **512**-**513**, **520**-**521** and **522**-**523**, with the output of the members of each pair preferably being added together by respective 54-bit adders **541**-**544** after the output of one member of pair has been shifted left 18 bits by respective shifter **55**. One or more of shifters **55** may be programmably bypassable (not shown) as in the embodiment of FIGS. **3** and **4**, above, but in this embodiment, for performing a 54-bit-by-54-bit multiplication, shifters **55** preferably are not bypassed (even if they are bypassable).

In the specialized processing block described in above-incorporated application Ser. No. 11/447,472, the output of adder **541**, and the output of adder **542** after being shifted left 18 bits by shifter **545**, would be added by 3:2 compressor **560** and chained carry/propagate adders **570**, **571**. Similarly, the outputs of adders **543** and **544** would be added by 3:2 compressor **561** and chained carry/propagate adders **572**, **573**. In accordance with the present invention, a 4:2 compressor **562** as well as two 36-bit right-shifters **546**, **547** are added. A number of AND gates **580**-**583** are added as selectors as described below, although multiplexers also could be used for that purpose, and AND gate **584** is added to chain together adders **570**, **571** with adders **572**, **573**. In addition, 18-bit right-shifter **548** and AND gate **585** are added, bridging half-blocks **52**, **53** which are in different specialized processing blocks. Note that a further 18-bit right-shifter (not shown) like shifter **548** and a further AND gate (not shown) like AND gate **585**, could connect half-block **51** to another half-block to the right (not shown) in a similar manner.

When not being used in the 54-bit-by-54-bit multiplication mode, each specialized processing block operates like that shown in above-incorporated application Ser. No. 11/447,472. As such, the second input (not shown) of each of AND gates **580**, **582**, **584** and **585** is a "0" so that shifters **546**-**548** are not in use and the carry/propagate adder chains of the two half-blocks remain separate. Similarly, the second input (not shown) of each of AND gates **581**, **583** is a "1" so that each partial product feeds directly into its respective 3:2 or 4:2 compressor. Note that in this case, with a "0" on the second input of AND gate **580**, 4:2 compressor **562** will act like a 3:2 compressor **560**, **561**.

When the specialized processing blocks are being used in the 54-bit-by-54-bit multiplication mode, the second input (not shown) of each of AND gates **580**, **582**, **584** and **585** is a "1" so that shifters **546**-**548** are in use and the carry/propagate adder chains of the two half-blocks are connected.

Because this is a 72-bit addition, the carry-out from 44-bit adder **571** to 44-bit adder **572** (via AND gate **584**) preferably is taken not from the end of adder **571**, but preferably from the 29th bit of adder **571**, which, including adder **570**, is the 73rd bit position, representing the carry-out from a 72-bit addition. Although it relies on more than one specialized processing block, this arrangement adds together all of the partial products substantially without resorting to general-purpose programmable logic of the PLD.

FIG. **6** shows schematically how 4:2 compressor **562** may be configured from two 3:2 compressors **560** (or **561**).

The invention will now be described with reference to FIGS. **7-9** in the context of a complex 36-by-18 multiplication, as well as a signed 54-bit-by-54-bit multiplication.

A 36-bit-by-18-bit complex multiplication can be broken down into eight 18-bit-by-18-bit multiplications, with appropriate shifters and adders. In accordance with this embodiment, all eight 18-but-by-18-bit multiplications and associated logic can be implemented in a single specialized processing block.

A 36-bit-by-18-bit complex multiplication can be decomposed as follows:

$$(A[35:0]+jC[35:0])\times(B[17:0]+jD[17:0])=(\{AH,AL\}+j\{CH,CL\})\times(B+jD)=((\{AH,AL\}\times B)-(\{CH,CL\}\times D))+j((\{AH,AL\}\times D)+(\{CH,CL\}\times B))=\text{Real: }[((AH\times B)<<18)+(AL\times B)]-[((CH\times D)<<18)+(CL\times D)]$$

$$\text{Imag: }[((AH\times D)<<18)+(AL\times D)]+[((CH\times B)<<18)+(CL\times B)]$$

The imaginary part may be implemented in embodiment **30** described above in FIG. **3**, using the two first level shifters **311**, **331**, and bypassing the second level shifter **37**. With regard to the real part, the subtraction required in the real part requires that signed multiplication be used. However, in the 36-bit-by-36-bit mode of embodiment **30**, the lower 18 bits of a 36-bit operand are always treated as unsigned regardless of the sign control signal, because the sign information is in the upper 18 bits. Thus, in FIG. **3**, the first multiplicand (A) of multiplier **32**, the second multiplicand (BH) of multiplier **33**, and both multiplicands (C, BL) of multiplier **34** are forced into unsigned mode. Therefore, embodiment **30** cannot compute the real part of a 36-bit-by-18-bit complex multiplication, nor can it compute the imaginary part if signed multiplication is required.

Embodiment **70** (FIG. **7**) can compute the real part of a 36-bit-by-18-bit complex multiplication, as well as the imaginary part if signed multiplication is required. For example, the real part can be rewritten as:

$$\text{Real: }[((AH\times B)<<18)+(AL\times B)]+[((CH\times(-D))<<18)+(CL\times(-D))]$$

In embodiment **70**, as in embodiment **30**, the two first level shifters **311**, **331** are used, and the second level shifter **37** is bypassed. In addition, at least the second multiplicands of multipliers **33** and **34** are not forced to unsigned mode, allowing the negated value of D to be input to those multipliers. This requires that the negation of D take place in other circuitry or in programmable logic of the PLD. The inputs to multipliers **33**, **34** can be made unforced by connecting a respective one of multiplexers **71**, **72** to the respective sign control inputs **73** of multipliers **33**, **34**, allowing each sign control input **73** to be connected either to ground (forced to unsigned) or to the sign control signal associated with the respective multiplicand.

In a further embodiment **80**, shown in FIG. **8**, which is an extension of embodiment **70**, all multiplicands have multiplexers **81** similar to multiplexers **71**, **72**, that allow any multiplicand either to be forced to be unsigned, or to be signed or unsigned according to an associated sign control signal. This would allow not only the implementation of a 36-bit-by-18-bit complex multiplication as described above, but also the implementation of a 54-bit-by-54-bit signed multiplication, whereas the 54-bit-by-54-bit multiplication described above is only an unsigned multiplication.

In embodiment **80**, signed 54-bit-by-54-bit multiplication can be implemented by applying appropriate control signals to force all the lower 18-bit multiplicands to be unsigned, while allowing the upper 18-bit multiplicands, which carry the sign information, to be signed. Similarly, in embodiment **80**, complex 36-bit-by-18-bit multiplication can be implemented by forcing all multiplicands to be signed except those noted above in connection with embodiment **70**.

Embodiment **80** also may be used to implement the entire real part of a complex multiplication without the external negation required in embodiment **70**. The real part can be rewritten:

$$\text{Real: }[((AH\times B)<<18)+(AL\times B)]+[((CH\times(-D))<<18)+(CL\times(-D))]=\text{Real: }[(AH\times B)-(CH\times D)]<<18+[(AL\times B)-(CL\times D)]$$

This can be implemented by embodiment **90** of FIG. **9**, bypassing the first-level shifters **311**, **331** and using the subtraction capability of adder/subtractors **350**, **351**, and also using second-level shifter **37**. For this embodiment **90**, the first multiplicand of multiplier **32** and the second multiplicand of multiplier **34** would have to be set not to be forced to be unsigned.

Embodiment **90**, with the first-level shifters bypassed, is similar to the specialized processing block/half-block of the PLD of the above-incorporated application Ser. No. 11/447,472, which does not have the shifters. This suggests that at least the first stage of a large multiplication such as a 36×18 complex multiplication can be carried out more efficiently in such a PLD if it is broken down mathematically as in embodiment **90**. This is illustrated as embodiment **100** of FIG. **10**, in which the first-stage multiplications are performed by multipliers **31-34** and then combined using adder/subtractors **350**, **351**. However, because the specialized processing block/half-block of the PLD of the above-incorporated application Ser. No. 11/447,472, illustrated in FIG. **10** at **111**, lacks the necessary shifter **37**, the shifting and further addition in embodiment **100** is carried out in programmable logic **112** of the PLD. Although embodiment **100** has been described as a 36×18 complex multiplication, because of limitations of the way that specialized processing block/half-block **111** forms the sum of two 18-bit-by-18-bit multiplications (as described in above-incorporated application Ser. No. 11/447,472), there is no provision for a carry-out bit, and therefore this embodiment actually is limited in that PLD to a 36×17 complex multiplication. However, in the specialized processing block/half-block of the aforementioned STRATIX® II PLD (or in the earlier STRATIX® PLD also available from Altera Corporation), this embodiment **100** could be used for a 36×18 complex multiplication.

Thus it is seen that a large multiplication that requires more than one specialized processing block of a PLD can be performed using fewer or no general-purpose programmable resources of the PLD.

A PLD **280** incorporating such circuitry according to the present invention may be used in many kinds of electronic devices. One possible use is in a data processing system **900** shown in FIG. **11**. Data processing system **900** may include one or more of the following components: a processor **281**; memory **282**; I/O circuitry **283**; and peripheral devices **284**. These components are coupled together by a system bus **285** and are populated on a circuit board **286** which is contained in an end-user system **287**.

System **900** can be used in a wide variety of applications, such as computer networking, data networking, instrumentation, video processing, digital signal processing, or any other application where the advantage of using programmable or

reprogrammable logic is desirable. PLD **280** can be used to perform a variety of different logic functions. For example, PLD **280** can be configured as a processor or controller that works in cooperation with processor **281**. PLD **280** may also be used as an arbiter for arbitrating access to a shared resources in system **900**. In yet another example, PLD **280** can be configured as an interface between processor **281** and one of the other components in system **900**. It should be noted that system **900** is only exemplary, and that the true scope and spirit of the invention should be indicated by the following claims.

Various technologies can be used to implement PLDs **280** as described above and incorporating this invention.

Instructions for carrying out the method according to this invention may be encoded on a machine-readable medium, to be executed by a suitable computer or similar device to implement the method of the invention for programming PLDs. For example, a personal computer may be equipped with an interface to which a PLD can be connected, and the personal computer can be used by a user to program the PLD using a suitable software tool, such as the QUARTUS® II software available from Altera Corporation, of San Jose, Calif.

FIG. **12** presents a cross section of a magnetic data storage medium **600** which can be encoded with a machine executable program that can be carried out by systems such as the aforementioned personal computer, or other computer or similar device. Medium **600** can be a floppy diskette or hard disk, or magnetic tape, having a suitable substrate **601**, which may be conventional, and a suitable coating **602**, which may be conventional, on one or both sides, containing magnetic domains (not visible) whose polarity or orientation can be altered magnetically. Except in the case where it is magnetic tape, medium **600** may also have an opening (not shown) for receiving the spindle of a disk drive or other data storage device.

The magnetic domains of coating **602** of medium **600** are polarized or oriented so as to encode, in manner which may be conventional, a machine-executable program, for execution by a programming system such as a personal computer or other computer or similar system, having a socket or peripheral attachment into which the PLD to be programmed may be inserted, to configure appropriate portions of the PLD, including its specialized processing blocks, if any, in accordance with the invention.

FIG. **13** shows a cross section of an optically-readable data storage medium **700** which also can be encoded with such a machine-executable program, which can be carried out by systems such as the aforementioned personal computer, or other computer or similar device. Medium **700** can be a conventional compact disk read only memory (CD-ROM) or digital video disk read only memory (DVD-ROM) or a rewriteable medium such as a CD-R, CD-RW, DVD-R, DVD-RW, DVD+R, DVD+RW, or DVD-RAM or a magneto-optical disk which is optically readable and magneto-optically rewriteable. Medium **700** preferably has a suitable substrate **701**, which may be conventional, and a suitable coating **702**, which may be conventional, usually on one or both sides of substrate **701**.

In the case of a CD-based or DVD-based medium, as is well known, coating **702** is reflective and is impressed with a plurality of pits **703**, arranged on one or more layers, to encode the machine-executable program. The arrangement of pits is read by reflecting laser light off the surface of coating **702**. A protective coating **704**, which preferably is substantially transparent, is provided on top of coating **702**.

In the case of magneto-optical disk, as is well known, coating **702** has no pits **703**, but has a plurality of magnetic domains whose polarity or orientation can be changed magnetically when heated above a certain temperature, as by a laser (not shown). The orientation of the domains can be read by measuring the polarization of laser light reflected from coating **702**. The arrangement of the domains encodes the program as described above.

It will be understood that the foregoing is only illustrative of the principles of the invention, and that various modifications can be made by those skilled in the art without departing from the scope and spirit of the invention. For example, the various elements of this invention can be provided on a PLD in any desired number and/or arrangement. One skilled in the art will appreciate that the present invention can be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims that follow.

What is claimed is:

1. For use in a programmable logic device having a plurality of specialized processing blocks, each of said specialized processing blocks having at least four n-by-n multipliers arranged in four-multiplier units, a method of performing a signed 3n-by-3n multiplication operation, said method comprising:

performing a 2n-by-2n multiplication using four of said n-by-n multipliers in a first of said four-multiplier units;

performing an n-by-n multiplication using one of said n-by-n multipliers in a second of said four-multiplier units; and

performing first and second 2n-by-n multiplications in a third of said four-multiplier units, using two of said n-by-n multipliers for each of said 2n-by-n multiplications; wherein:

in each of said multiplications, multiplicands representing n most significant bits are treated as signed operands and multiplicands representing n least significant bits are forced to be unsigned; said method further comprising:

shifting a second partial product of each of said 2n-by-n multiplications to align it with a first partial product of each of said 2n-by-n multiplications for addition within said third four-multiplier unit; and

adding results of said multiplications from said first, second and third four-multiplier units.

2. The method of claim **1** wherein said adding comprises adding said results in general-purpose programmable logic of said programmable logic device.

3. The method of claim **2** wherein:

said performing first and second 2n-by-n multiplications comprises, for each respective one of said first and second 2n-by-n multiplications:

performing a respective most significant bit multiplication using one said multiplier in said third four-multiplier unit to form a respective most significant bit partial product, and

performing a respective least significant bit multiplication using another said multiplier in said third four-multiplier unit to form a respective least significant bit partial product;

said shifting comprises shifting each respective most significant bit partial product to the left without shifting either respective least significant bit partial product; and

said addition within said third four-multiplier unit excludes further shifting of partial products.

4. The method of claim **3** further comprising selecting control signals to perform said shifting and said addition without further shifting.

5. The method of claim **1** wherein each said specialized processing block comprises two said four-multiplier units.

6. A programmable logic device having a plurality of specialized processing blocks, each of said specialized processing blocks having at least four n-by-n multipliers arranged in four-multiplier units, said programmable logic device being configured to perform a signed 3n-by-3n multiplication operation and comprising:

four of said n-by-n multipliers in a first of said four-multiplier units configured to perform a 2n-by-2n multiplication;

one of said n-by-n multipliers in a second of said four-multiplier units configured to perform an n-by-n multiplication;

a third of said four-multiplier units configured to perform first and second 2n-by-n multiplications, using two of said n-by-n multipliers for each of said 2n-by-n multiplications;

circuitry at multiplicand inputs of at least one of said multipliers for selectably forcing at least one of said inputs to be unsigned;

a shifter configured to shift a second partial product of each of said 2n-by-n multiplications to align it with a first partial product of each of said 2n-by-n multiplications for addition within said third four-multiplier unit; and

circuitry configured to add results of said multiplications from said first, second and third four-multiplier units.

7. The configured programmable logic device of claim 6 wherein said adding comprises adding said results in general-purpose programmable logic of said programmable logic device.

8. The configured programmable logic device of claim 7 wherein:

said programmable logic device is configured to perform said first and second 2n-by-n multiplications by, for each respective one of said first and second 2n-by-n multiplications:

performing a respective most significant bit multiplication using one said multiplier in said third four-multiplier unit to form a respective most significant bit partial product, and

performing a respective least significant bit multiplication using another said multiplier in said third four-multiplier unit to form a respective least significant bit partial product;

said programmable logic device is configured to shift each respective most significant bit partial product to the left without shifting either respective least significant bit partial product; and

said circuitry configured to add excludes further shifting of partial products.

9. The configured programmable logic device of claim 8 further comprising selectors responsive to selection control signals to perform said shifting and said addition without further shifting.

10. The configured programmable logic device of claim 6 wherein each said specialized processing block comprises two said four-multiplier units.

11. The configured programmable logic device of claim 10 wherein said circuitry configured to add is located substantially within one said specialized processing block.

12. The configured programmable logic device of claim 6 wherein said circuitry for selectably forcing at least one of said inputs to be unsigned comprises a multiplexer at said multiplicand input, said multiplexer controllably selecting, for input to a sign control input associated with said multiplicand input, between a first signal forcing said multiplicand input to be unsigned, and a second signal representing sign information for said multiplicand input.

13. The configured programmable logic device of claim 6 wherein said circuitry for selectably forcing at least one of said inputs to be unsigned comprises one said multiplexer at at least one multiplicand input of each said multiplier.

14. The configured programmable logic device of claim 13 wherein said circuitry for selectably forcing at least one of said inputs to be unsigned comprises one said multiplexer at each multiplicand input of each said multiplier.

15. A data storage medium encoded with machine-executable instructions for performing a method of programmably configuring a programmable logic device to perform a signed 3n-by-3n multiplication operation, wherein said programmable logic device has a plurality of specialized processing blocks, each of said specialized processing blocks having at least four n-by-n multipliers arranged in four-multiplier units, said instructions comprising:

instructions for configuring four of said n-by-n multipliers in a first of said four-multiplier units to perform a 2n-by-2n multiplication;

instructions for configuring one of said n-by-n multipliers in a second of said four-multiplier units to perform an n-by-n multiplication;

instructions for configuring a third of said four-multiplier units to perform first and second 2n-by-n multiplications, using two of said n-by-n multipliers for each of said 2n-by-n multiplications;

instructions for configuring multiplicand inputs in any of said multiplications to be selectably treatable as signed operands or unsigned operands;

instructions for configuring a shifter to shift a second partial product of each of said 2n-by-n multiplications to align it with a first partial product of each of said 2n-by-n multiplications for addition within said third four-multiplier unit; and

instructions for configuring circuitry to add results of said multiplications from said first, second and third four-multiplier units.

16. The data storage medium of claim 15 wherein said instructions for configuring circuitry to add comprise instructions for configuring general-purpose programmable logic of said programmable logic device to add said results.

17. The data storage medium of claim 16 comprising:

instructions to configure said programmable logic device to perform said first and second 2n-by-n multiplications including, for each respective one of said first and second 2n-by-n multiplications:

instructions to configure said programmable logic device to perform a respective most significant bit multiplication using one said multiplier in said third four-multiplier unit to form a respective most significant bit partial product, and

instructions to configure said programmable logic device to perform a respective least significant bit multiplication using another said multiplier in said third four-multiplier unit to form a respective least significant bit partial product; and

instructions to configure said programmable logic device to perform to shift each respective most significant bit partial product to the left without shifting either respective least significant bit partial product; wherein:

said instructions to configure said circuitry to add excludes further shifting of partial products.

18. The data storage medium of claim 17 wherein said instructions further comprise instructions to configure selectors responsive to selection control signals to perform said shifting and said addition without further shifting.

19. The data storage medium of claim 15 wherein said instructions are for configuring a programmable logic device wherein each said specialized processing block comprises two said four-multiplier units.

20. The data storage medium of claim 19 wherein said instructions configure said circuitry to add substantially within one said specialized processing block.

21. The data storage medium of claim 15 wherein said instructions for configuring multiplicand inputs in any of said multiplications to be selectably treatable as signed operands or unsigned operands include instructions for configuring a respective multiplexer at each respective said multiplicand input, each said respective multiplexer being configured to controllably select, for input to a sign control input associated with said respective multiplicand input, between a first signal forcing said multiplicand input to be unsigned, and a second signal representing sign information for said multiplicand input.

* * * * *